CLAIMS

What is claimed:

1. A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:
initiating formation of the nitride/high-k material/nitride gate dielectric stack by depositing a first ultra-thin nitride film on a semiconductor substrate;
depositing a high-k material on the first ultra-thin nitride film;
depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure;
completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and
completing fabrication of the device.

2. A method as recited in claim 1, wherein the substrate comprises a silicon wafer or a silicon-on-insulator (SOI) wafer.

3. A method as recited in claim 1,
wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and
wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and
wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

4. A method as recited in claim 1, wherein the high-k material comprises a thin metal film.

5. A method as recited in claim 1, wherein the thin metal film comprises at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta).

6. A method as recited in claim 1, wherein the thin metal film comprises a metal oxide.

7. A method as recited in claim 1,
wherein the second ultra-thin nitride film is deposited using an atomic layer deposition (ALD) technique, and
wherein the second ultra-thin nitride film comprises silicon nitride (Si_3N_4), and
wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

8. A method as recited in claim 1, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:
depositing a thick gate material on the second ultra-thin nitride film;
patterning the thick gate material, thereby forming a gate electrode; and
etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack

9. A method as recited in claim 1, wherein completing fabrication of the device comprises forming of a MOSFET structure comprising the gate dielectric stack.

10. A method as recited in claim 8,
wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and
wherein the thick gate material is patterned using a material such as photoresist.

11. A method as recited in claim 1, wherein completing fabrication of the device comprises:
forming a source/drain structure in the substrate and flanking the gate dielectric stack;
forming at least one spacer on at least one sidewall of the gate dielectric stack; and

silicidizing a shallow source/drain region as well as the high-k gate stack, thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

12. A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:

initiating formation of the nitride/high-k material/nitride gate dielectric stack by depositing a first ultra-thin nitride film on a semiconductor substrate,

wherein the substrate comprises a silicon wafer or a silicon-on-insulator (SOI) wafer;

depositing a high-k material on the first ultra-thin nitride film;

depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure;

completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and

completing fabrication of the device.

13. A method as recited in claim 12,

wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and

wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and

wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

14. A method as recited in claim 13,
wherein the high-k material comprises a thin metal film,
wherein the thin metal film comprises at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta), and
wherein the thin metal film comprises a metal oxide.

15. A method as recited in claim 14,
wherein the second ultra-thin nitride film is deposited using an atomic layer deposition (ALD) technique, and
wherein the second ultra-thin nitride film comprises silicon nitride (Si_3N_4), and
wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

16. A method as recited in claim 15, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:
depositing a thick gate material on the second ultra-thin nitride film;
patterning the thick gate material, thereby forming a gate electrode; and
etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack

17. A method as recited in claim 16, wherein completing fabrication of the device comprises forming of a MOSFET structure comprising the gate dielectric stack.

18. A method as recited in claim 17,
wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and
wherein the thick gate material is patterned using a material such as photoresist.

19. A method as recited in claim 18, wherein completing fabrication of the device

comprises:

forming a source/drain structure in the substrate and flanking the gate dielectric stack;

forming at least one spacer on at least one sidewall of the gate dielectric stack; and

silicidizing a shallow source/drain region as well as the high-k gate stack, thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

20. A semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:

a first ultra-thin nitride film deposited on a semiconductor substrate;

a high-k material deposited on the first ultra-thin nitride film;

a second ultra-thin nitride film deposited on the high-k material, thereby forming a sandwich structure; and

the nitride/high-k material/nitride gate dielectric stack formed from the sandwich structure.